REMARKS

In response to the Advisory Action dated March 19, 2002, Applicants respectfully request consideration of the remarks which follow.

I. Claims Rejected Under 35 U.S.C. §112, second paragraph

The Examiner rejects Claim 17 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Regarding Claim 17, the Examiner contends that it is unclear which materials have a work function corresponding to P-type silicon and which have a work function corresponding to N-type silicon. In response, Applicants note that the work functions of the materials in Claim 17 are well-known to those in the art. As one example, see the attached table entitled Electron Work Functions of the Elements beginning on page E-89 in the *CRC Handbook of Chemistry and Physics* (67th Ed.).

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II. Claims Rejected Under 35 U.S.C. § 102(b)

The Examiner rejects Claims 1-2 and 16 under 35 U.S.C. § 102(b) as being anticipated by Dash et al, U.S. Patent No. 4,399,605 ("Dash"). Applicants respectfully traverse this rejection.

In order to anticipate a claim, the relied upon reference must disclose every limitation of the claim. Among other limitations, Claim 1 (as amended) recites that the first metal gate electrode and the second metal gate electrode are each separately disposed in respective ones of the first area and the second area of the semiconductor substrate.

In making the rejection, the Examiner relies on Dash to show a circuit device comprising two metal gate electrodes 56 and 50. (*See* Dash, Fig. 9.) The Examiner argues that the first metal gate electrode (a portion of layer 56 formed above channel region 52) and the second metal gate electrode 50 are separately disposed in respective ones of a first area (P-type region 52) and a second area (N-type region 54) of the semiconductor substrate. However, Applicants note that metal gate electrode 56 is formed above both P-type region 52 and N-type region 54 of the semiconductor substrate since the conductive line 56 acts as the gate electrode for the N channel transistor and as a contact with the platinum silicide gate electrode 50 of the P channel transistor. (*See* Dash, Fig. 9, col. 4, lines 17-21.) Thus, Dash fails to teach or suggest that the first metal gate electrode and the second metal gate electrode are each separately disposed in respect of ones of a first area and a second area of the semiconductor substrate.

III. Claims Rejected under 35 U.S.C. §103(a)

The Examiner rejects Claim 17 under 35 U.S.C. §103(a) as being obvious over Dash. Applicants respectfully traverse this rejection.

The Examiner's obligation in making a *prima facie* case of obviousness requires the Examiner to show that the prior art, in combination, teaches or suggests all elements of the claimed invention. Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness.

Claim 17 depends from independent Claim 1. As argued above, Dash fails to teach or suggest that the first metal gate electrode and the second metal gate

electrode are each separately disposed in respective ones of the first area and the second area of the semiconductor substrate.

Thus, Claim 17 is not anticipated for at least the same reasons as independent Claim 1.

CONCLUSION

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 4/3/02

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on 4/3, 2002.

Diane Martinez 4/3/02
Date

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended as follows:

1. (Twice Amended) A circuit device comprising:

a first transistor including a first metal gate electrode over a first gate dielectric on a first area of a semiconductor substrate and having a work function corresponding to the work function of one of P-type silicon and N-type silicon;

a second transistor complementary to the first transistor including a second metal gate electrode over a second gate dielectric on a second different area of a semiconductor substrate and having a work function corresponding to the work function of the other one of P-type silicon and N-type silicon; and

wherein the first metal gate electrode and the second metal gate electrode are each separately disposed in respective ones of the first area and the second area of the semiconductor substrate.